ABSTRACT

A process for making improved borderless contact structure to salicide field effect transistors (FETs) has been achieved. Salicide FETs are formed on device areas surrounded by a shallow trench isolation (STI) using a first rapid thermal anneal (RTA-1) to form a metal silicide on the source/drain contacts and the gate electrodes, and a second rapid thermal anneal (RTA-2) is delayed until after forming a borderless contact opening structures to the source/drain areas of the FETs. An etch stop (Si3N4) layer and an interlevel dielectric (ILD) layer is deposited, and borderless contact openings, extending over the STI, are etched in the ILD and etch stop layers to the source/drain areas. The contact openings across the substrate must be overetched to insure that all contacts are open. This results in overetched region in the STI at the source/drain-STI interface that result in source/drain-to-substrate shorts when metal plugs are formed in the contact openings. This invention uses a contact opening implant to dope and modified the junction profile in the source/drain contact around the STI over etched region to prevent electrical shorts. The second RTA (RTA-2) is then used to concurrently reduce the silicide sheet resistance and to electrically activate the contact opening implanted dopant. Metal plugs can now be formed without causing shorts.